ABSTRACT OF THE DISCLOSURE

The present technique relates to a method and apparatus for managing voltage buses. In a memory device, such as SRAM or DRAM, a periphery voltage bus may supply voltage to periphery circuitry and an array voltage bus may supply voltage to array circuitry. A bridge circuit may be utilized to isolate the buses from each other and couple the buses together, depending on the control signals are received by the bridge circuit. As such, the bridge circuit enhances the operation of the memory device by reducing duplicative circuits and equalizing the voltage that are applied to the buses. In addition, the bridge circuit isolates the buses from each other to protect sensitive circuitry in the array and periphery circuitry from noise on the other bus.